What is claimed is:

Sub A'

1. A transistor comprising:

a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type provided on said semiconductor layer and an oppositely conductive region of a second conductivity type provided on said drain layer;

a trench provided such that it extends from a surface of said oppositely conductive region to said drain layer;

a source region of the first conductivity type provided in said oppositely conductive region and exposed on an inner circumferential surface of said trench;

a gate insulating film provided on the inner circumferential surface and inner bottom surface of said trench such that it reaches to said drain layer, said oppositely conductive region and said source region;

a gate electrode material provided in tight contact with said gate insulating film;

a source electrode film provided in contact with at least said source region exposed on the inner circumferential surface of said trench and electrically insulated from said gate electrode material.

2. A transistor according to Claim 1, further comprising a drain electrode film formed on a surface of said semiconductor

layer opposite to said drain layer.

3. A transistor according to Claim 1, wherein the impurity concentration of said semiconductor layer is higher than the impurity concentration of said drain layer.

4. A transistor according to Claim 1, further comprising an insulating material thicker than said gate insulating film provided between said gate electrode material in said trench and said source electrode film.

5. A transistor according to Claim 4, wherein said insulating material is any one of a silicon oxide film, a combination of a silicon oxide film and PSG film, a combination of silicon oxide film and a BPSG film, and a combination of a silicon oxide film and a silicon nitride film.

6. A transistor according to Claim 4, wherein said insulating material has a thickness between 0.01 μm and 1.0 μm inclusive.

Sub A2

7. A transistor according to Claim 5, wherein said insulating material has a thickness between 0.01 μm and 1.0 μm inclusive.

8. A transistor according to Claim 1, wherein said trench is provided in the form of a mesh on a top surface of said semiconductor substrate and wherein said source region is provided in contact with said trench.

9. A transistor according to Claim 1, wherein said semiconductor layer is of the first conductivity type.

10. A transistor according to Claim 1, wherein said semiconductor layer is of the second conductivity type as opposed to said drain layer.

11. A transistor comprising:

a semiconductor substrate having a drain layer of a first conductivity type and an oppositely conductive region of a second conductivity type provided on said drain layer;

a trench provided such that it extends from a surface of said oppositely conductive region to said drain layer;

a source region of the first conductivity type provided in said oppositely conductive region and exposed on an inner circumferential surface of said trench;

a gate insulating film provided on the inner circumferential surface and inner bottom surface of said trench such that it reaches to said drain layer, said oppositely conductive region and said source region;

a gate electrode material provided in tight contact with said gate insulating film;

a source electrode film provided in contact with at least said source region exposed on the inner circumferential surface of said trench and electrically insulated from said gate electrode material; and

a metal film formed on a surface of said drain layer opposite to said oppositely conductive region to establish Schottky contact with said drain layer.

12. A method of manufacturing a transistor, comprising the steps of:

diffusing an impurity on a top surface of a drain layer of a first conductivity type provided on a semiconductor layer to form an oppositely conductive region of a second conductivity type;

etching a top surface of said oppositely conductive region to form a trench whose inner bottom surface is located lower than an upper end of said drain layer;

forming a gate insulating film at least on an inner circumferential surface of said trench;

forming a gate electrode material whose upper end is higher than a lower end of said oppositely conductive region in said trench;

forming a source region which is in contact with said

gate insulating film and whose lower end is lower than the upper end of said gate electrode material in said oppositely conductive region;

forming an insulating material whose upper end is lower than the opening of said trench on said gate electrode material; and

forming a source electrode film in contact with said source region with at least a top surface of said source region exposed.

13. A method of manufacturing a transistor according to Claim 12, wherein the top surface of said source region and an inner circumferential surface of said trench in the vicinity of the opening thereof are exposed when said source electrode film is formed.

14. A method of manufacturing a transistor according to Claim 12, wherein said step of forming said insulating material includes the steps of:

forming a first insulating film on a top surface of said gate electrode material, an inner circumferential surface of said trench in the vicinity of the opening thereof and a top surface of said oppositely conductive region;

forming a second insulating film on a top surface of said first insulating film to fill the interior of said trench; and

etching said first and second insulating films to leave said first and second insulating films such that upper ends thereof are lower than the opening of said trench.

15. A method of manufacturing a transistor according to Claim 14, wherein said step of forming said gate electrode material includes the step of depositing polysilicon in said trench and wherein said step of forming said first insulating film includes the step of oxidizing a top surface of said gate electrode film, an inner circumferential surface of said trench in the vicinity of the opening thereof and a top surface of said oppositely conductive region to form said first insulating film.

add C3